* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The process which forms at least one or more cascade screens including the structure which comes to insert the upper and lower sides of the electric conduction film used as a gate electrode by the insulator layer on a semi-conductor substrate, The process which processes this cascade screen in the shape of an island, and the process which forms the 1st diffusion field in the substrate front face of said cascade screen bottom, The process which carries out etching removal and forms opening until a substrate front face exposes the center section of said cascade screen, The manufacture approach of the semiconductor device characterized by having the process which embeds the semi-conductor film as a barrier layer at said opening circles, and the process which forms the 2nd diffusion field in the upper part of this semi-conductor film after forming gate dielectric film in the side attachment wall of these opening circles.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the semiconductor device equipped with the vertical mold MOS transistor.
[0002]
[Description of the Prior Art] SGT (Surrounding GateTransistor) is known as one of the switching elements of the conventional memory cell. The configuration of the conventional SGT is shown in drawing 12 . This drawing (a) is a perspective view of SGT. Moreover, this drawing (b) is a sectional view which cut SGT of this drawing (a) at the flat surface perpendicular to a substrate front face including Point A and A'.
[0003] This SGT is explained according to a production process. First, p mold well 121 is formed in the front face of a silicon substrate 120. Next, the silicon column 122 is formed by performing anisotropic etching, such as RIE, as well as formation of the usual trench to p mold well 121.
[0004] Next, after forming gate oxide 123 in the whole surface, the polish recon film used as the gate electrode 124 is deposited on the whole surface, and the gate electrode 124 is formed in the side face of the Si column 122 by carrying out anisotropic etching of this polish recon film by RIE etc.
[0005] Finally, an ion implantation is used and the diffusion layer 125 used as n mold source and a drain is formed in a substrate front face and a silicon column top face. A perpendicular NAND memory cell is obtained by carrying out series connection of such SGT in the direction perpendicular to a substrate front face. It is necessary to form two or more gate electrodes 124 each other insulated by the silicon column 122 for realizing this.
[0006] However, in order to realize such structure, after depositing the polish recon film used as the gate electrode 124 on the whole surface, a part of this polish recon film is removed, it separates into two or more silicon film, and the difficult process of embedding an insulator layer into the part removed further is required. For this reason, by the conventional manufacture approach, forming a perpendicular NAND memory cell had the problem of being difficult.
[0007]
[Problem(s) to be Solved by the Invention] Like ****, forming perpendicularly the perpendicular NAND mold memory cell which comes to carry out series connection of two or more SGT(s) to a substrate front face had the problem of being difficult, by the conventional manufacture approach.
[0008] This invention was made in consideration of the above-mentioned situation, and the purpose is in offering the manufacture approach of the semiconductor device which can form easily perpendicularly the component structure which comes to carry out series connection of two or more vertical mold MOS transistors to a substrate front face.
[0009]
[Means for Solving the Problem]
[Elements of the Invention] -- the manufacture approach of the semiconductor device concerning this invention, in order to attain the account purpose of a top The process which forms at least one or more

cascade screens including the structure which comes to insert the upper and lower sides of the electric conduction film used as a gate electrode by the insulator layer on a semi-conductor substrate, The process which processes this cascade screen in the shape of an island, and the process which forms the 1st diffusion field in the substrate front face of said cascade screen bottom, The process which carries out etching removal and forms opening until a substrate front face exposes the center section of said cascade screen, After forming gate dielectric film in the side attachment wall of these opening circles, it is characterized by having the process which embeds the semi-conductor film as a barrier layer at said opening circles, and the process which forms the 2nd diffusion field in the upper part of this semi-conductor film.

[0010] The concrete gestalt of this invention is as follows.

(1) if a flat-surface pattern forms in a cascade screen opening which has the pattern which does not divide said cascade screen -- a gate electrode -- a conductor -- the vertical mold MOS transistor (SGT) of the structure surrounding a membranous perimeter can be formed.

(2) If a flat-surface pattern forms in a cascade screen opening which has the pattern which divides said cascade screen, a vertical mold transistor can be formed in the side attachment wall in opening which carries out phase opposite, respectively. In other words, a vertical mold MOS transistor can be formed in two fields as for which a cascade screen carries out phase opposite, respectively.

(3) As gate dielectric film, the memory cell of the NAND mold EEPROM can be formed by using that threshold electrical potential differences differ by the existence of a charge using the insulator layer which can carry out the trap of the charges, such as a cascade screen of silicon rich silicon oxide, and silicon oxide / silicon nitride / silicon oxide, and a cascade screen of a silicon nitride / silicon oxide. Moreover, the ferroelectric film may be used as gate dielectric film. In this case, it uses that threshold electrical potential differences differ in the state of polarization of the ferroelectric film.

[0011] (Operation) By the conventional manufacture approach, after forming a semi-conductor column, two or more gate electrodes each other divided into the perimeter by the insulator layer were formed. [each other]

[0012] On the other hand, in this invention, the cascade screen which first includes the structure which comes to insert the upper and lower sides of the electric conduction film as a gate electrode by the insulator layer is formed. Therefore, when a cascade screen including two or more above-mentioned structures is formed, two or more gate electrodes of each other will already be separated by the insulator layer in this phase. Next, in this invention, opening which arrives at a substrate front face in the above-mentioned cascade screen is formed, and these opening circles are embedded by the semi-conductor film as a semi-conductor column (barrier layer) after an appropriate time.

[0013] Thus, since it is not necessary to use the difficult process of removing some electric conduction film used as two or more gate electrodes formed in the side face of a semi-conductor column, and embedding this removed part by the insulator layer according to the invention in this application, the component structure which comes to carry out series connection of two or more vertical mold MOS transistors can be perpendicularly formed easily to a substrate front face.

[0014]

[Embodiment of the Invention] Hereafter, the gestalt (henceforth an operation gestalt) of operation of this invention is explained, referring to a drawing.

(1st operation gestalt) Drawing 1 - drawing 3 are the process sectional views showing the manufacture approach of the n channel vertical mold transistor (SGT) concerning the 1st operation gestalt of this invention.

[0015] The description of the manufacture approach of this operation gestalt is to form a silicon column (barrier layer), after forming a gate electrode contrary to the conventional approach. First, sequential formation of silicon oxide 11, the polish recon film 12 used as a gate electrode, and the silicon oxide 13 is carried out on a silicon substrate 10. Silicon oxide 11 and 13 is SiO2. It is the film. Then, the photoresist pattern 14 which has the pattern which specifies the gate field of a transistor and a silicon column field is formed on silicon oxide 13 (drawing 1 (a)). Here, a flat-surface pattern uses a rectangular thing as a photoresist pattern 14.

[0016] Next, the photoresist pattern 14 is used for a mask, anisotropic etching of the cascade screens 13-11 is carried out to this order, and the pattern of the photoresist pattern 14 is imprinted to cascade screens 13-11. Then, n mold diffusion layer 15 is formed in the front face of the silicon substrate 10 of the cascade screen 13-11 bottom using ion-implantation (drawing 1 (b)). Next, a top face is higher than silicon oxide 13, and forms the silicon nitride 16 as a wrap component demarcation membrane in the whole surface for cascade screens 11-13 (drawing 1 (c)). The silicon nitride 16 is Si3 N4. It is the film.
[0017] Next, the front face of the silicon nitride 16 makes it retreat, and flattening of the front face is carried out until it becomes the same height as the front face of silicon oxide 13 using polish or etchback of CMP etc. (drawing 1 (d)).
[0018] Next, in order to expose the center section of the cascade screens 11-13 in the shape of a rectangle, the photoresist pattern 17 is formed on the silicon nitride 16 and silicon oxide 16 (drawing 2 (e)). This photoresist pattern 17 defines the field (active region) of a silicon column. In addition, you may be a stripe-like thing like the 2nd operation gestalt described later.
[0019] Next, the photoresist pattern 17 is used for a mask, and cascade screens 11-13 are etched until a substrate front face is exposed (drawing 2 (f)). Consequently, the opening 18 of the shape of the method object of merit or a cube is formed.
[0020] Next, gate dielectric film 19 is formed in the whole surface. At this time, gate dielectric film 19 is thinly formed so that opening 18 may not be embedded (this drawing (f)). Specifically, it is about 6-50nm. As the formation approach of gate dielectric film 19, the polish recon film is deposited on the whole surface, and the approach of oxidizing this polish recon film and the approach of depositing and forming a silicon oxide are raised, for example.
[0021] Next, the protective coat 20 which consists of direct polish recon or an amorphous silicon is formed in the whole surface (drawing 3 (g)). At this time, a protective coat 20 is thinly formed so that opening 18 may not be embedded. This protective coat 20 is for protecting the gate dielectric film 19 in opening 18 in the case of etching of a back process.
[0022] Next, the protective coat 20 of the bottom of opening 18 and the gate dielectric film 19 under it are removed using an anisotropic etching technique (drawing 3 (h)). Next, after removing a protective coat 18, the silicon film 21 used as the silicon column (barrier layer) of a transistor is embedded in opening 18. At this time, the silicon film 21 is thickly formed so that the whole surface may be covered (drawing 3 (i)).
[0023] Here, although the protective coat 18 was removed, you may leave. The silicon film 21 is the polycrystal film formed for example, by the depositing method, the amorphous silicon film, or silicon film formed on the silicon substrate 10 by the selection epitaxial grown method. Although which type of undoping, n mold, and p mold is sufficient as the silicon film 21, in the case of an n-type channel, it is usually p mold.
[0024] n mold diffusion layer 22 which uses ion-implantation and finally serves as one side of the source and a drain on the top face of the silicon film 21 is formed (this drawing (i)). Here, distance between n mold diffusion layer 22 and the polish recon film 12 is set to about 6-50nm. When using this component for a memory cell, patterning of the n mold diffusion layer 22 is carried out, and a bit line is formed.
[0025] In addition, although n mold diffusion layer 15, the silicon film 21 and n mold diffusion layer 22, and the silicon film 21 are physically separated, respectively, since both the thickness of gate dielectric film and the distance between n mold diffusion layer 22 and the silicon film 21 are the small values of about 6-50nm, when the gate voltage more than a threshold electrical potential difference is impressed, n mold diffusion layer 15 and n mold diffusion layer 22 are connected electrically. In addition, n mold diffusion layer 22 may be formed in the depth of extent which laps with the gate electrode 12.
[0026] Moreover, to use this SGT as a non-volatile memory cell, it is necessary to use the insulator layer which has the property stated with the 2nd operation gestalt as gate dielectric film 19.
[0027] As stated above, the cascade screen which sandwiched the upper and lower sides of the electric conduction film 12 used as a gate electrode by insulator layers 11 and 13 according to this operation gestalt is formed, and SGT can be formed now by the new method of removing the center section of this

cascade screen after an appropriate time, and embedding the silicon film 12 after an appropriate time. (2nd operation gestalt) Drawing 4 is drawing showing the memory array of the perpendicular NAND mold EEPROM concerning the 2nd operation gestalt of this invention. Drawing 4 (a) is a top view and 4 Figs. (b) are view A-A'sectional views of this drawing (a). The NAND mold EEPROM is the thing of the structure where what connected to the serial two or more FET mold MOS memory cells which have charge accumulation layers, such as a cascade screen of a nitride or a floating gate, for an oxide film was connected to the bit line in the end as one cel unit here. With this operation gestalt, the thing of a configuration of having carried out series connection of the three vertical mold MOS transistors perpendicularly to the substrate front face as a memory cell is used.

[0028] Among drawing, 40 show the silicon substrate and arrangement formation of the n mold source drain diffusion layer 41 is carried out in the front face of this silicon substrate 40 at two or more parallel. On the both ends of n mold source drain diffusion layer 41, the laminated structure of the 46/polish recon film 47 of 45/silicon oxide of 43/silicon oxide of silicon oxide of 44/polish recon film of 42/polish recon film is formed, respectively. The polish recon film 43, 45, and 47 serves as a gate electrode of each transistor, respectively. Hereafter, the structure where the laminating of the polish recon film (gate electrode) and the insulator layer was carried out by turns in this way is called laminating gate structure.

[0029] The silicon nitride 49 as a spacer is formed on laminating gate structure. On n mold source drain diffusion layer 41 of the field across which it faced by the silicon nitride 49 formed two adjoining laminating gate structures and on it, the silicon nitride 48 as a component demarcation membrane is formed so that between these may be filled.

[0030] Moreover, gate dielectric film 50 is formed in the side attachment wall of the opening 50 of the field across which it faced by the silicon nitride 49 formed two adjoining laminating gate structures and on it. Opening 30 is embedded by the polish recon film 52 as a silicon column (barrier layer), and n mold source drain diffusion layer 53. n mold source drain diffusion layer 53 is a bit line and really formed. The bit line is formed so that it may intersect perpendicularly with n mold source drain diffusion layer 41.

[0031] In addition, both the thickness of silicon oxide 42, 44, and 46 and the distance between n mold source drain diffusion layer 53 and the silicon film 52 are about 6-50nm in small value. If it is thickness of this level, even if it will not form n mold diffusion layer in the polish recon film 52, a current flows between n mold source drain diffusion layer 41 and 53. Therefore, even if there is no n mold diffusion layer, the perpendicular NAND mold memory cell by which the vertical mold MOS transistor was connected to the serial is realized.

[0032] Next, the manufacture approach of the memory cell constituted in this way is explained. The process sectional view in which drawing 5 - drawing 8 show the manufacture approach of this semiconductor device, and drawing 9 are the process top views showing the manufacture approach of this semiconductor device.

[0033] First, sequential formation of silicon oxide 42, the polish recon film 43, silicon oxide 44, the polish recon film 45, silicon oxide 46, the polish recon film 47, and the silicon oxide 54 (laminating gate structure) is carried out on a silicon substrate 40 (drawing 5 (a)).

[0034] In this phase, the polish recon film 43, 45, and 47 as a gate electrode is mutually separated by silicon oxide 44 and 46. Moreover, the polish recon film 43 and a silicon substrate 40 are separated by the polish recon film 42.

[0035] Next, the photoresist pattern 55 for specifying the gate field of a transistor and a silicon column field is formed on silicon oxide 54 (drawing 5 (a), drawing 9 (a)). Here, the pattern of the photoresist pattern 55 is a stripe pattern as shown in drawing 5 (a).

[0036] next -- until it uses a photoresist 55 for a mask and a substrate front face is exposed -- laminating gate structure 42- anisotropic etching of 47 and 54 is carried out. consequently, laminating gate structure 42- 47 and 54 are divided by stripe-like opening. Next, n mold impurity is doped on the exposed substrate front face, and n mold source drain diffusion layer 41 is formed in it (drawing 5 (b)). The polish recon film 43, 45, and 47 which remained without carrying out etching removal at this process serves as a gate electrode (word line).

[0037] next, a top face -- silicon oxide 54 -- high -- laminating gate structure 42- the silicon nitride 48 as a wrap component demarcation membrane is formed in the whole surface for 47 and 54 (drawing 5 (c)).

[0038] Next, the front face of the silicon nitride 54 makes it retreat, and flattening of the front face is carried out until it becomes the same height as the front face of silicon oxide 54 using polish or etchback of CMP etc. (drawing 5 (d)).
[0039] Next, silicon oxide 54 is removed (the silicon nitride 49 which carries out, and serves as a spacer (etching mask) continuously is formed in the whole surface (.)) (drawing 6 (f)). (drawing 6 (e)) Next, the photoresist pattern 60 for specifying the active region of a transistor is formed on silicon oxide 54 (drawing 9 (b)). As drawing 9 (a) and drawing 9 (b) show, the pattern of the photoresist pattern 60 is a stripe pattern which crosses perpendicularly to the photoresist pattern 55.
[0040] Next, the photoresist pattern 60 is used for a mask, and anisotropic etching of the silicon nitride 49 is carried out until the polish recon film 47 is exposed (drawing 7 (g), drawing 9 (c)). Consequently, the spacer which becomes the side attachment wall of the silicon nitride 48 from the silicon nitride 49 is formed.
[0041] Next, the silicon nitride 49 (spacer) and the silicon nitride 48 are used for a mask, and the laminating gate structures 42-47 are etched until a substrate front face is exposed (drawing 7 (h)). Consequently, the stripe-like opening 50 is formed in self align. In addition, the thickness and the etching conditions of the silicon nitride 49 are chosen at the process of drawing 6 (f) and drawing 7 (g) so that n mold source drain diffusion layer 41 may not be exposed at the process of this drawing 7 (h).
[0042] Moreover, opening may be formed using the same pattern as the 1st operation gestalt, i.e., the photoresist pattern which has the pattern which the center section of laminating gate structure exposes in the shape of a rectangle. In this case, three SGT(s) by which series connection was perpendicularly carried out to the substrate front face are obtained.
[0043] Next, thin gate dielectric film 51 is formed in the whole surface. Gate dielectric film 19 deposits and forms for example, a silicon oxide. Moreover, it may oxidize and the front face of the polish recon film 43, 45, and 47 in opening 50 may be formed. In this case, gate dielectric film 51 is not formed in the whole surface, but is formed only in the front face of the polish recon film 43, 45, and 47 in opening 50.
[0044] Here, in order for information to be statically memorizable, gate dielectric film 51 must have the capacity which accumulates a charge. The threshold of a transistor is changed with the amount of the charge accumulated, and binary data are distinguished by change of the threshold electrical potential difference of a transistor.
[0045] As gate dielectric film which has the capacity which accumulates a charge, the laminating membrane structure of the cascade screen of silicon rich silicon oxide, and silicon oxide / silicon nitride / silicon oxide, or a silicon nitride / silicon oxide is raised, for example.
[0046] Since the trap of the electron is carried out for gate dielectric film 51 to the interface of silicon nitriding and silicon oxide in the case of the laminating membrane structure of silicon oxide / silicon nitride / silicon oxide, and silicon nitriding / silicon oxide and a threshold electrical potential difference changes, EEPROM actuation is attained.
[0047] Moreover, the ferroelectric film may be used as gate dielectric film 51. In this case, a charge is not accumulated, but an electrical potential difference is impressed to a gate electrode, polarization of the ferroelectric film is carried out, and the threshold electrical potential difference of a transistor is changed. If positive voltage is impressed to gate voltage, a channel side polarizes in plus. Even after this polarization condition cancels impression of gate voltage, it is maintained. Therefore, since the electron density of a channel becomes high in this condition, a threshold electrical potential difference falls. On the contrary, if a minus electrical potential difference is impressed to a gate electrode, since a channel side will polarize in minus and the electron density of a channel will become low, a threshold electrical potential difference becomes high.
[0048] Next, the protective coat 56 which becomes the whole surface from polish recon or an amorphous silicon is formed in the whole surface (this drawing (i)). This protective coat 56 is for

protecting in the case of etching of a back process, so that the gate dielectric film 51 in opening 50 may not be etched.
[0049] Next, the protective coats 56 and gate dielectric film 51 other than the side attachment wall of opening 50 are removed using an anisotropic etching technique (drawing 7 (j)). Next, opening 50 is embedded with the silicon film 52 (drawing 8 (k)). The upper part of this silicon film 52 serves as n mold source drain diffusion layer 53 and a bit line, and the part under it is used as a silicon column (barrier layer).
[0050] Next, n mold impurity is doped on the front face of the silicon film 52 using an ion implantation, and n mold source drain diffusion layer 53 is formed (this drawing (k)). Distance between n mold source drain diffusion layer 53 and the polish recon film (gate electrode) 47 is set to about 6-50nm as mentioned above. In addition, n mold source drain diffusion layer 53 may be formed in the depth of extent which laps with the gate electrode 47.
[0051] Finally patterning of the polish recon film 53 with which n mold impurity was doped is carried out, and the bit line BL which intersects perpendicularly in the direction which a gate electrode (word line) runs is formed (drawing 9 (d)). The perspective view of this phase is shown in drawing 11 . In addition, the insulator layer is omitted.
[0052] As stated above, after according to this operation gestalt forming laminating gate structure and forming the gate electrodes 43, 45, and 47 each other separated by the insulator layer by carrying out patterning of this, the memory cell which comes to carry out series connection of the three vertical mold MOS transistors can be perpendicularly formed easily to a substrate front face by forming the silicon film (silicon column) 52 in opening 50.
[0053] Furthermore, in the case of this operation gestalt, the gate electrodes 43, 45, and 47 do not surround the whole perimeter of the silicon film (silicon column) 52. The gate electrodes 43, 45, and 47 are formed in the 2nd page in which the silicon film 52 carries out phase opposite. Consequently, two NAND mold memory cells electrically divided into one polish recon film (barrier layer) 52 are formed. Therefore, according to this operation gestalt, a memory cell advantageous to high integration can be realized now.
[0054] The sectional view of the memory cell of the conventional NAND mold EEPROM is shown in drawing 10 as an example of a comparison. Four memory transistors which consist of double gate structures of the control gate CGi and a floating gate FGi (i=1-4) are connected to the serial in the level direction to the substrate front face.
[0055] These four memory transistors are pinched by the gate electrode SGj and two selection transistors which consist of SGj' (1 j= 2). Moreover, n mold source drain diffusion layer SDk (k=1-7) of the above-mentioned transistor is formed in the front face of p mold well layer 101 formed in the front face of n mold silicon substrate 100. In addition, 102 shows an insulator layer and 103 shows the bit line.
[0056] Supposing the gate length of a memory transistor and a selection transistor is L, he is [spacing between L (design rule) and the adjoining transistor of memory cell die length] 12L. In addition, the bit line contact field is not taken into consideration among n mold source drain diffusion layers SD 1 here.
[0057] Moreover, supposing the width of face of the active region of a memory cell is L and the width of face of the component isolation region between two NAND cels is also L, the width of face of a memory cell is 2L. Therefore, the area (cel area) which one memory cell occupies is 12Lx2L=24L2. It becomes.
[0058] On the other hand, according to the NAND mold EEPROM according to a **** gestalt, the cel area is made as follows. Width of face of a word line and width of face of the isolation region between word lines are set to L, and width of face of a bit line and spacing of a bit line are also set to L. Thus, by designing, it is cel area 2Lx2L=4L2 It can carry out. That is, it ends with one sixth of the cel area of the example of a comparison, and is very advantageous to high integration. Moreover, since the vertical mold MOS transistor is used as a memory transistor with this operation gestalt, the above-mentioned cel area value is fixed regardless of the number of memory transistors.
[0059] What is necessary is to form the cascade screen of x(an insulator layer / polish recon film) six,

and just to use the gate electrode of a selection transistor, and other polish recon film of four layers for the polish recon film of the maximum upper layer and the lowest layer as a gate electrode of four memory transistors as laminating gate structure, in order to realize a 4-bit perpendicular NAND mold memory cell like the example of a comparison.

[0060] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, although the above-mentioned operation gestalt explained the case of an n-type channel transistor, it is applicable also to p mold channel transistor by making reverse conductivity types, such as a source drain diffusion layer.

[0061] Moreover, although the above-mentioned operation gestalt explained the case of EEPROM, applying also to DRAM also becomes possible by using the usual insulator layer which does not have charge storage capacity as gate dielectric film. In addition, it is the range which does not deviate from the summary of this invention, and it is possible to deform variously and to carry out.

[0062]

[Effect of the Invention] Component structure which comes to carry out series connection of two or more vertical mold MOS transistors perpendicularly to a substrate front face can be easily realized now by according to this invention, carrying out the laminating of an insulator layer and the electric conduction film as a gate electrode by turns, forming opening in this cascade screen, as explained in full detail above, and forming a semi-conductor column in these opening circles.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The process sectional view showing the manufacture approach of the vertical mold MOS transistor concerning the 1st operation gestalt of this invention
[Drawing 2] The process sectional view showing the manufacture approach of the vertical mold MOS transistor concerning the 1st operation gestalt of this invention
[Drawing 3] The process sectional view showing the manufacture approach of the vertical mold MOS transistor concerning the 1st operation gestalt of this invention
[Drawing 4] Drawing showing the configuration of the NAND cel using the vertical mold MOS transistor concerning the 2nd operation gestalt of this invention
[Drawing 5] Drawing showing the memory array of the perpendicular NAND mold EEPROM concerning the 2nd operation gestalt of this invention
[Drawing 6] The process sectional view showing the manufacture approach of the memory cell array of drawing 4
[Drawing 7] The process sectional view showing the manufacture approach of the memory cell array of drawing 4
[Drawing 8] The process sectional view showing the manufacture approach of the memory cell array of drawing 4
[Drawing 9] The process top view showing the manufacture approach of the memory cell array of drawing 4
[Drawing 10] The sectional view showing the memory cell array of the conventional NAND mold EEPROM
[Drawing 11] The perspective view of the memory cell array of the 2nd operation gestalt
[Drawing 12] Drawing showing the configuration of the conventional SGT
[Description of Notations]
10 -- Silicon substrate
11 13 -- Silicon oxide
12 -- Polish recon film
14 -- Photoresist pattern
15 -- n mold diffusion layer (1st diffusion field)
16 -- Silicon nitride
17 -- Photoresist pattern
18 -- Opening
19 -- Gate dielectric film
20 -- Protective coat
21 -- p mold polish recon film
22 -- n mold diffusion layer (2nd diffusion field)
40 -- Silicon substrate
41 -- n mold source drain diffusion layer (1st diffusion field)

42, 44, 46, 54 -- Silicon oxide
43, 45, 47 -- Polish recon film
48 -- Silicon nitride (demarcation membrane)
49 -- Silicon nitride (spacer)
50 -- Opening
51 -- Gate dielectric film
52 -- p mold polish recon film
53 -- n mold source drain diffusion layer (2nd diffusion field)
55 -- Photoresist pattern
56 -- Protective coat

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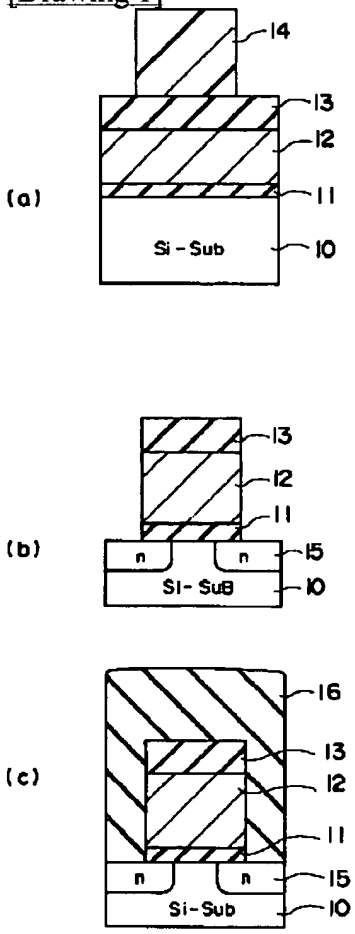
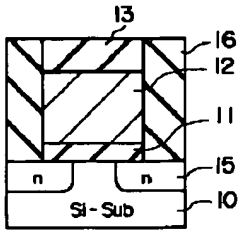
DRAWINGS

[Drawing 1]



[Drawing 2]

(d)



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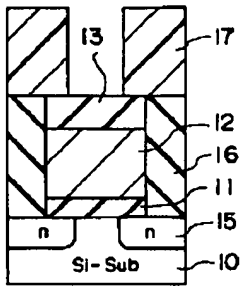
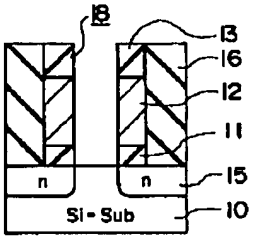
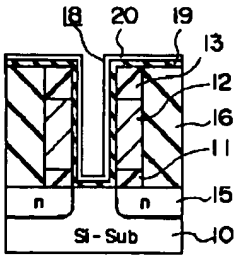


(f)

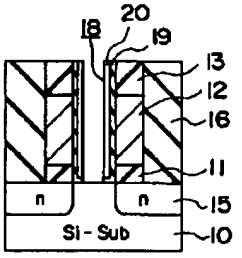


[Drawing 3]

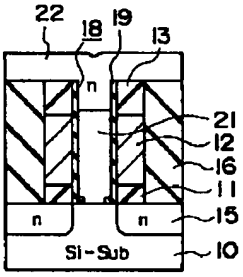
(g)



(h)

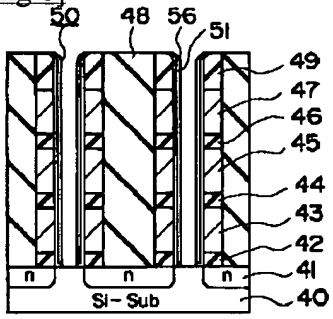


(i)

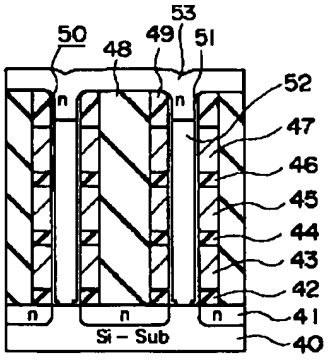


[Drawing 8]

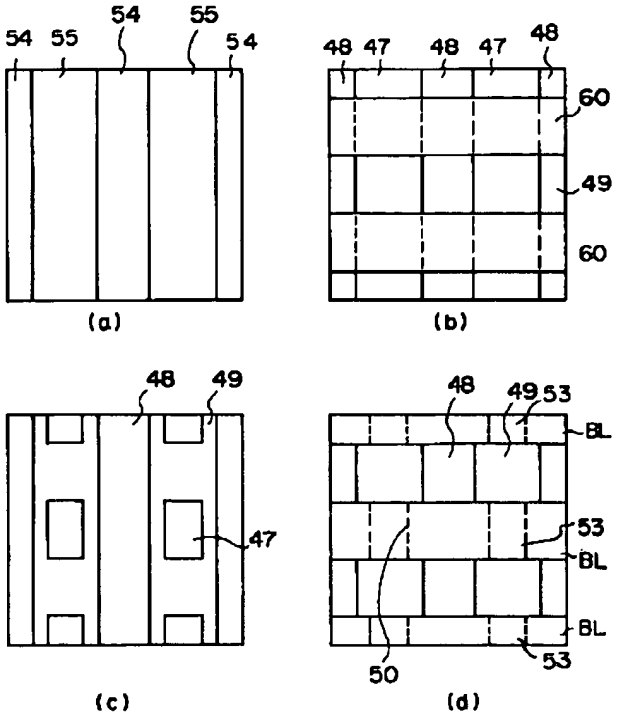
(j)



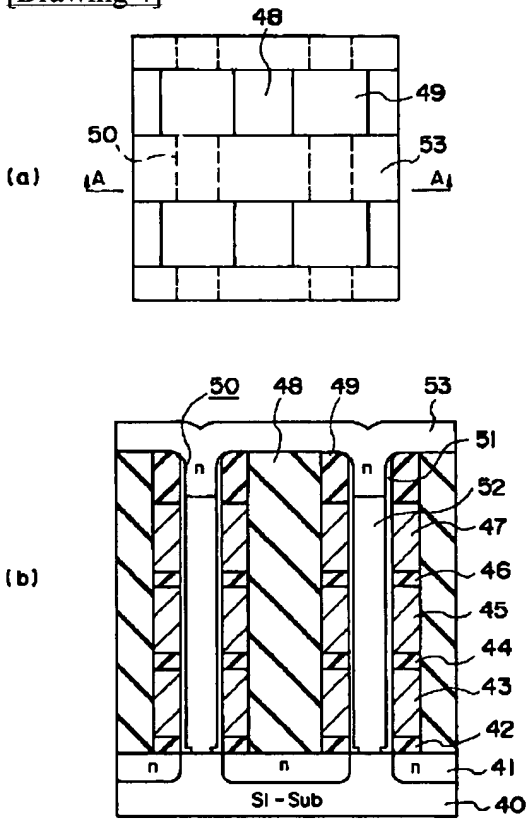
(k)



[Drawing 9]

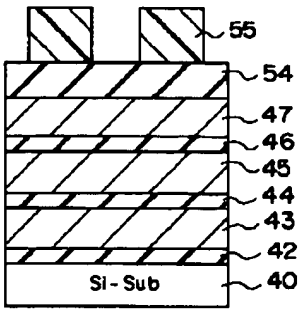


[Drawing 4]

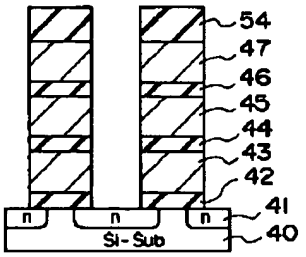


[Drawing 5]

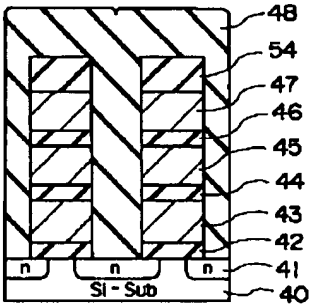
(a)



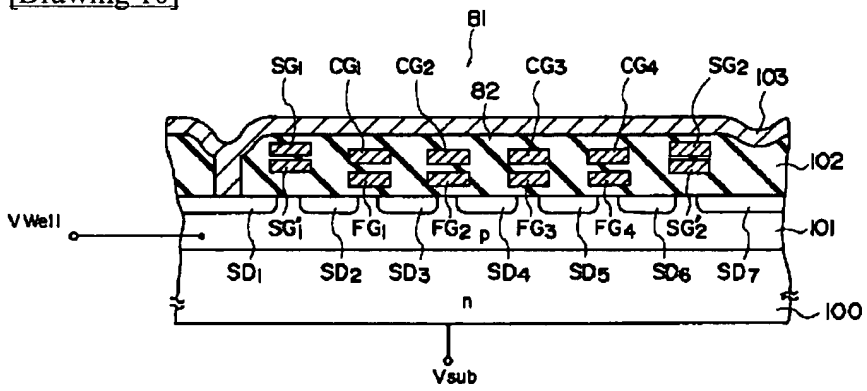
(b)



(c)

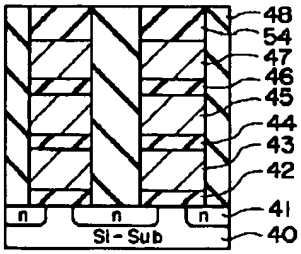


[Drawing 10]

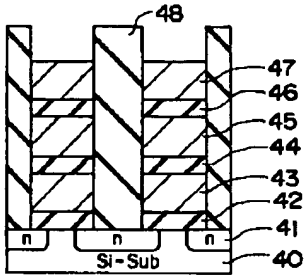


[Drawing 6]

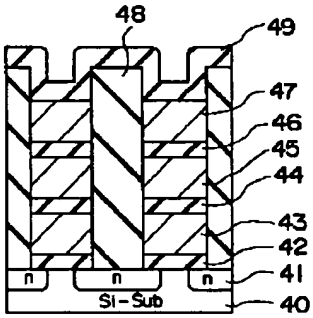
(d)



(e)

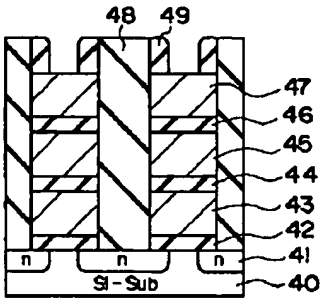


(f)

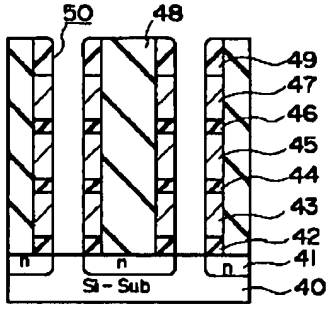


[Drawing 7]

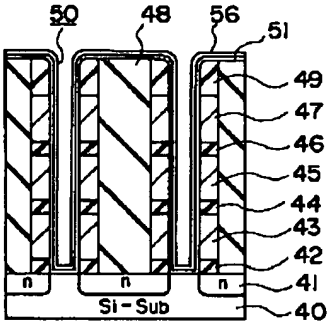
(g)



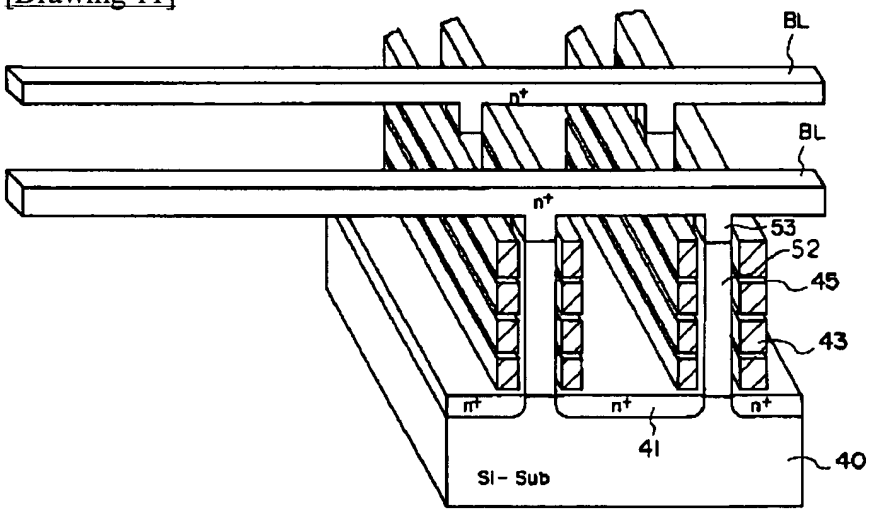
(h)



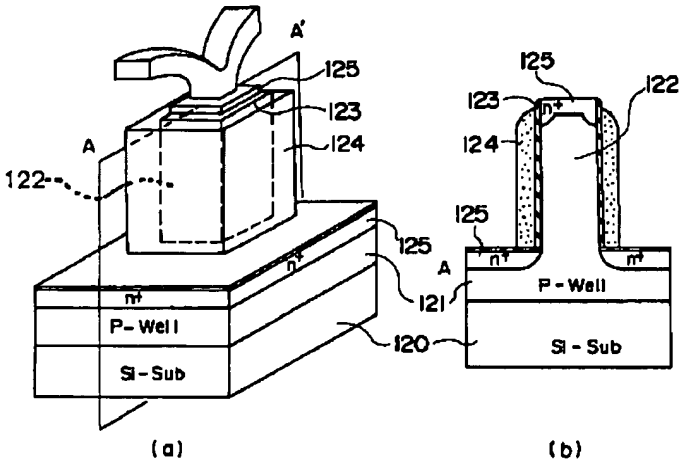
(i)



[Drawing 11]



[Drawing 12]



[Translation done.]